PROGRAM
M. Tech.
VLSI Design

Department of Electronics and Communication Engineering

CURRICULUM AND SYLLABUS

(From 2018 Admission Onwards)

Contents

Vision of the Institute

To be a global leader in the delivery of engineering education, transforming individuals to become creative, innovative, and socially responsible contributors in their professions.

Mission of the Institute:

- To provide best-in-class infrastructure and resources to achieve excellence in technical education,
- To promote knowledge development in thematic research areas that have a positive impact on society, both nationally and globally,
- To design and maintain the highest quality education through active engagement with all stakeholders –students, faculty, industry, alumni and reputed academic institutions,
- To contribute to the quality enhancement of the local and global education ecosystem,
- To promote a culture of collaboration that allows creativity, innovation, and entrepreneurship to flourish, and
- To practice and promote high standards of professional ethics, transparency, and accountability.

Vision of the Department:

To provide a value-based learning environment for producing engineers with a blend of technical skills, moral values and leadership qualities in the field of Electronics, Communication and Computing channelized towards technological advancement to cater to the needs of the industry and the society.

Mission of the Department:

M1: Achieving excellence in teaching and learning with an emphasis on fundamental knowledge and hands-on exposure to match the state-of-the-art in technology.
M2: Providing an environment for core competency development and enhancing quality research in emerging areas.
M3: Facilitating professional growth to the students for higher education and career in industry and academia.
M4: Imbibing the essence of human values, ethics and professional skills to sustain socio-economic development.

The Program Educational Objectives (PEOs)

- **PEO1** : Attain mastery in applying VLSI concepts to Engineering problems so as to meet the need of the industry, teaching, higher education or research.
- **PEO2** : Creation of expertise in the microelectronics domain to deal with design, development, analysis, testing and evaluation of the critical aspects of integrated circuits and its core concepts.
- **PEO3** : To exhibit professional competence and leadership qualities with harmonious blend of ethics leading to an integrated personality development.

Programme Outcomes

- Creation of expertise and work force in the microelectronics domain to deal with design, development, analysis, testing and evaluation of the critical aspects of integrated circuits and its core concepts to cater to the requirements of the industry and academia.
- Facilitate research opportunities in the integrated circuits domain aimed at developing state-of the art technologies with value based social responsibility.
- Developing professional competence in microelectronics domain and leadership qualities with a harmonious blend of ethics leading to an integrated personality development.

Curriculum Structure

First semester

Course code	Type	Course	L T P	Cr
18MA602	FC	Mathematical Methods for Engineering *(Common for VLSI Design, Communication Engineering & Signal Processing and Biomedical Engineering)*	302	4
18VL601	FC	Graph Theory and Applications	2 0 0	2
18VL602	FC	Physics and Technology of MOS Devices	3 0 0	3
18VL611	SC	CMOS Integrated Circuits	3 1 0	4
18VL612	SC	Digital System Design	3 0 0	3
18VL613	SC	Analog IC Design	3 0 2	4
18VL631	SC	VLSI Design Laboratory – I	0 04	2
18HU601	HU	Amrita Values Program*		P/F
18HU602	HU	Career Competency I*		P/F
		Credits		**22**

* Non-credit course

Second Semester

Course code	Type	Course	L T P	Cr
18VL614	SC	Design Verification	3 0 0	3
18VL615	SC	VLSI Signal Processing	3 0 0	3
18VL616	SC	Design for Test and Testing	3 0 0	3
	E	Fractal Elective I	1 0 0	1
	E	Fractal Elective II	1 0 0	1
	E	Fractal Elective III	1 0 0	1
	E	Live-in Lab/Elective I	3 0 0	3
	E	Elective II/ Open Elective**	3 0 0	3
18VL632	SC	VLSI Design Laboratory –II	0 02	1
18RM600	SC	Research Methodology	2 0 0	2
18HU603	HU	Career Competency II	0 02	1
		Credits		**22**

** Courses can also be taken from other departments

Third semester

Course code	Type	Course	L T P	Cr
18VL798	P	Dissertation		10
		Credits		**10**

Fourth Semester

Course code	Type	Course	L T P	Cr
18VL799	P	Dissertation		10
		Credits		**10**
		TOTAL CREDITS (22+22+10+10)		**64**

L- Lecture; T-Tutorial; P-Practical

FC- Foundation Core; SC- Subject Core; E-Electives; P- Dissertation; P/F- Pass/Fail

List of Courses

Foundation Core

Course code	Course	L T P	Cr
18MA602	Mathematical Methods for Engineering *(Common for VLSI Design,Communication Engineering & Signal Processing and Biomedical Engineering)*	3 02	4
18VL601	Graph Theory and Applications	2 0 0	2
18VL602	Physics and Technology of MOS Devices	3 0 0	3

Subject Core

Course code	Course	L T P	Cr
18VL611	CMOS Integrated Circuits	3 1 0	4
18VL612	Digital System Design	3 0 0	3
18VL613	Analog IC Design	3 0 2	4
18VL614	Design Verification	3 0 0	3
18VL615	VLSI Signal Processing	3 0 0	3
18VL616	Design for Test and Testing	3 0 0	3
18VL631	VLSI Design Laboratory – I	0 04	2
18VL632	VLSI Design Laboratory –II	0 02	1
18RM600	Research Methodology	2 0 0	2

Elective Courses

Analog Circuits and Devices		**L T P**	**Cr**
18VL701	VLSI Signal Conditioning	3 0 0	3
18VL702	Semiconductor Memory Design	3 0 0	3
18VL703	Optoelectronic Devices	3 0 0	3
18VL704	Mixed Signal VLSI Design	3 0 0	3
Testing and Verification			
18VL711	VLSI Hardware Security and Trust	3 0 0	3
18VL712	Static Timing Analysis	3 0 0	3
18VL713	Design for Manufacturability	3 0 0	3
18VL714	Formal Verification	3 0 0	3
Computational VLSI			
18VL721	Computer Aided Design of VLSI Circuits	3 0 0	3
18VL722	Physical Design of Integrated Circuits	3 0 0	3
18VL723	Emerging Architectures for Machine Learning	3 0 0	3
18VL724	Wavelets and Applications	3 0 0	3
18VL725	Data Structures and Algorithms	3 0 0	3
Architecture			
18VL731	VLSI Architectures for Multi-Core and Heterogeneous Computing	3 0 0	3
18VL732	Hardware Software Co-Design	3 0 0	3

18VL733	Reconfigurable Computing	3 0 0	3
18VL734	Electronic System Level Design	3 0 0	3
18VL735	Low Power VLSI Circuits	3 0 0	3
18VL736	Network on Chip	3 0 0	3
Cyber Physical Systems			
18VL741	Embedded System Design	3 0 0	3
18VL742	FPGA Based System Design	3 0 0	3
18VL743	Cryptography	3 0 0	3
RF Integrated Circuits			
18VL751	CMOS RFIC Design	3 0 0	3
18VL752	Communication Systems and Networks	3 0 0	3
Technology			
18VL761	Nano Electronics	3 0 0	3
18VL762	VLSI Fabrication Technology	3 0 0	3
18VL763	Electronic Packaging and Reliability	3 0 0	3
18VL764	MEMS Design and Fabrication	3 0 0	3

Fractal Elective Courses

Analog Circuits and Devices		**L T P**	**Cr**
18VL771	Analog Layout	1 0 0	1
18VL772	Feedback Amplifiers	1 0 0	1
18VL773	Analog Filters	1 0 0	1
18VL774	Phase Locked Loops	1 0 0	1
Testing and Verification			
18VL775	Built-in Self Test	1 0 0	1
Computational VLSI			
18VL776	Deep Learning Techniques	1 0 0	1
18VL777	Internet of Things	1 0 0	1
RF Integrated Circuits			
18VL778	Low Noise Amplifier Design	1 0 0	1
18VL779	Oscillator Design	1 0 0	1
18VL780	Signal Integrity	1 0 0	1
Technology			
18VL781	FINFET Architecture	1 0 0	1
18VL782	Gallium Nitride Devices	1 0 0	1

Evaluation Pattern and Grading Scheme

50:50 (Internal: External) (All Theory Courses)

Assessment	Internal	External
Periodical 1 (P1)	15	
Periodical 2 (P2)	15	
*Continuous Assessment (CA)	20	
End Semester		50

80:20 (Internal: External) (Lab courses and Lab based Courses having 1 Theory hour)

Assessment	Internal	External
*Continuous Assessment (CA)	80	
End Semester		20

70:30(Internal: External) (Lab based courses having 2 Theory hours/ Theory and Tutorial) Theory- 60 Marks; Lab- 40 Marks

Assessment	Internal	External
Periodical 1	10	
Periodical 2	10	
*Continuous Assessment (Theory) (CAT)	10	
Continuous Assessment (Lab) (CAL)	40	
End Semester		30

65:35 (Internal: External) (Lab based courses having 3 Theory hours/ Theory and Tutorial) Theory- 70 Marks; Lab- 30 Marks

Assessment	Internal	External
Periodical 1	10	
Periodical 2	10	
*Continuous Assessment (Theory) (CAT)	15	
Continuous Assessment (Lab) (CAL)	30	
End Semester		35

*CA – Can be Quizzes, Assignment, Projects, and Reports.

Letter Grade	Grade Point	Grade Description
O	10.00	Outstanding
A+	9.50	Excellent
A	9.00	Very Good
B+	8.00	Good
B	7.00	Above Average
C	6.00	Average
P	5.00	Pass
F	0.00	Fail

Grades O to P indicate successful completion of the course

$$CGPA = \frac{\sum_i (C_i \times Gr)}{\sum C_i}$$

Where

C_i= Credit for the i^{th} course in any semester

Gr_i= Grade point for the i^{th} course

Cr. = Credits for the Course

Gr. = Grade Obtained

Syllabi and Course Outcomes

18MA602 MATHEMATICAL METHODS FOR ENGINEERING3-0-2-4

(Common for VLSI Design,Communication Engineering& Signal Processing and Biomedical Engineering)

Objectives:

- To introduce the mathematical methods applied for VLSI, signal processing and communication systems.
- To provide a unified applied treatment of fundamental mathematics, seasoned with demonstrations using standard tools.
- To develop contemporary techniques for applications in the diverse areas to improvethe analytical skills.
- To comprehend the computational concepts learned in mathematical methods through numerical simulations and programming.

Keywords: Linear Algebra, Matrix Decompositions, Optimization, Random Process.

Contents:

Matrices and vectors – inverse and transpose – vector spaces – subspaces – linear independence – basis and dimension – orthogonal vectors and subspaces – matrix decompositions – QR decomposition- Singular value decomposition – Eigen values – Eigen vectors – Diagonalization of matrix.

Introduction to Optimization - linear optimization – unconstrained optimization – constrained optimization – nonlinear optimization.

Introduction to Probability concepts- Two dimensional jointly distributed random variables, stochastic random variables, convergence and limit theorems, multi variant probability distribution covariance, and regression models. Bayesian methods of estimation.Random process, power spectrum, discrete time process, spectrum estimation.

Lab component: Gram Schmidt orthonormalization on vector spaces, Solving a system of linear equations using QR decomposition , Image compression using Singular value decomposition, Computation of basis for four fundamental subspaces for a given system ,Optimization using Newton's method with line search and Broydens update.

Outcomes:

CO1 Understanding the mathematical methods and applying it to practical problems by investigating from different perspectives.

CO2 Enabling an analytical approach towards developing mathematical models in various domains.

CO3 To develop competency in implementation of algorithms and numerical analysis.

TEXT BOOKS / REFERENCES:

1. Gilbert Strang, *Linear Algebra and its Applications*, Fourth Edition, Cambridge University Press. 2009.
2. Todd K. Moon and Wynn C. Sterling, *Mathematical Methods and Algorithms for Signal Processing*, PHI, 2000.
3. C. Bender and S. Orszag, *Advanced Mathematical Methods for Scientists and Engineers,* Springer, 1998.
4. Papoulis. A and S.U. Pillai*, Probability Random Variables and Stochastic Processes,*
5. Fourth Edition, McGraw Hill, 2002.

18VL601 GRAPH THEORY AND APPLICATIONS 2-0-0-2

Objective:

- To understand the basic concepts in graph theory.

Contents:

Graph Theory: Basic Definitions and Examples – Trees and their Characterization – Euler Circuits – Long Paths and Cycles – Vertex Colourings – Edge Colourings – Vizing's Theorem – Planar Graphs – Including Euler's Formula– Dual Graphs -Data structures for graph representations – Applications in CAD for VLSI- Algorithms - Spanning tree algorithms and shortest path algorithms.

Outcomes:

CO1 Apply graph theory concepts in VLSI Design.
CO2 Enable an analytical approach for circuit design.

TEXT BOOKS / REFERENCES:

1. NarasinghDeo, *Graph Theory with Applications to Engineering and Computer Science*, PHI Learning Pvt Ltd, 2004.
2. Gerez, *Algorithms for VLSI Design Automation*, John Wiley & Sons 2000.
3. NaveedSherwani, *Algorithms for VLSI Physical Design Automation*, Second Edition, Kluwer Academic Publishers, 1995.

18VL602 PHYSICS AND TECHNOLOGY OF MOS DEVICES 3-0-0-3

Objectives:

- Understanding the basic semiconductor device physics of PN junctions.
- To understand operational principles of MOSFET.
- Understand the evolution of MOSFET structure and Technology.
- Understand the basic working of FinFETs.
- Use of MOSFET models directly into the circuit simulators for Analog/RFDigital systems.

Keywords:MOSFET, MOSCAP, Sub-Threshold,MOS Gate Stack, High-k dielectrics, Metal Gate Electrodes, Strained Silicon, Silicon-on-Insulator,FinFET.

Contents:

Review of Basic Semiconductor Physics – Doping and Carrier Concentration-Femi Energy-Drift and Diffusion Currents-Transport Equation –Introduction to pn junction-built-in potential in equilibrium – Forward and Reverse Bias conditions – PN Junction Capacitance.

The ideal MOS Capacitor –Effect of Real Surfaces-MOSCAP Characteristics –MOSFET Characteristics-Threshold Voltage-Mobility-Substrate Bias –MOS Gate leakage - MOSFET parasitic capacitances-small signal model- Sub-threshold Characteristics - MOSFET Scaling and Short-channel Effects-DIBL, GIDL, Hot Carrier Effects

MOSFET structure evolution – High-k dielectrics, Metal Gate Electrodes, High mobility substrates (Strained Si, Ge), Elevated S/D - Silicon-on-Insulator structures – Ultra Shallow Junctions – Multiple Gate MOSFETs – Double Gate -Overview of CMOS Process flow-FinFETstructures and Operation – FinFET characteristics.

Outcomes:

CO1 Understand working principles of MOSFET and evolution of MOSFET structure.
CO2 Ability to use the MOSFET for DC, I-V, CV characteristics and in Analog/RF Circuit simulations.
CO3 Understanding principles of FinFET structures.

TEXT BOOKS/REFERNCES:

1. D.A.Neamen,*Semiconductor Physics and Devices: Basic Principle,* Third Edition, McGraw – Hill International,2003.
2. B.G Streetman and S.K Banerjee, *Solid State Electronic Devices,* Seventh Edition,PrenticeHall India,2010.
3. Y.Taur and T.H. Ning, *Fundamentals ofModern VLSI Devices,* Second Edition, Cambridge University Press,2009.
4. J. P. Collinge, *FinFETs and Other Multi-Gate Transistors,* Springer, 2008
5. SudebDasgupta, Brajesh Kumar Kaushik, Pankaj Kumar Pal Spacer, *Engineered FinFET Architectures: High-Performance Digital Circuit Applications,* CRC Press 2017.
6. S.M Sze and K.K Ng,*Physics of Semiconductor Devices,* Third Edition, John Wiley and Sons Inc.,2007.

18VL611 CMOS INTEGRATED CIRCUITS 3-1-0-4

Objectives:

- To introduce the basic concepts of MOS transistors.
- To provide a platform for transistor level digital circuits design.
- To learn and practice different logical implementation and their significances.

Keywords: PMOS, NMOS, Static, Transmission Gates, Switching Threshold, Rise/Fall Time, Delay, Sizing, Pseudo, Dynamic, Logical Effort.

Contents:

NMOS and PMOS Transistors – Threshold Voltage – Body Effect – Second-order Effects – NMOS and CMOS Inverters – Inverter Ratio.

DC and Transient Characteristics – Switching Times – Driving Large Capacitance Loads – CMOS Logic Structures – Transmission Gates – Static CMOS Design – Dynamic CMOS Design – Parasitic Estimation – Switching Characteristics.

Transistor Sizing – Power Dissipation and Design Margin – Charge Sharing – Logical Effort – Scaling – Combinational Circuits. Interconnects – Electro static discharge (ESD) – Latch-up and its Prevention – Introduction to Sequential Circuit Design and Timing Analysis.

Outcomes:

CO1 Ability to design basic digital circuits in transistor level.
CO2 Ability to choose the suitable logical styles for the given problems.
CO3 Ability to analyse the transistor level circuits.
CO4 Ability to measure delay and find optimized delay.

TEXT BOOKS / REFERENCES:

1. Jan M. Rabaey, Anantha P. Chandrakasan and BorivojeNikolić, *Digital Integrated Circuits: A Design Perspective*, Second Edition, Prentice Hall India, 2003.
2. Sung-Mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits - Analysis and Design*, Third Edition, Tata McGraw-Hill, 2003.
3. Neil H. E. Weste and David Money Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Fourth Edition, Addison Wesley, 2010.

18VL612 DIGITAL SYSTEM DESIGN 3-0-0-3

Objectives:

- To understand different logic and arithmetic functional units and their design.
- To design and synthesize FSMs and data path and control path.
- To learn asynchronous circuits and their design principles.
- Learn and apply hardware Description Language (Verilog) and SoC design flow.

Keywords: Shift Registers, Memory, Multiplier, Finite State Machine, Arithmetic Processor, Data path, Control path, Asynchronous circuits, Approximate Logic.

Contents:

Register Files – FIFOs – LIFOs – SIPOs – Bidirectional Shift Register – Universal Shift Register – Barrel Shifter – Linear Feedback Shift Registers – Memory – RAM – Static RAM – Dynamic RAM – Serial Access Memory – ROM – Content Addressable Memory – Booth Multiplier – Wallace Tree Multiplier – Baugh-Wooley Multiplier.

Design and Synthesis of Data Path Controller – State Diagram to Control External Hardware Subsystems and Synthesis – Synchronous and Asynchronous FSM Design – Programmable Logic and Storage – Algorithm and Architecture for Digital Arithmetic Processor Design –Post Synthesis Design.

Principles of Asynchronous Interaction – Handshake Protocols –Muller C Element – Simple Pipelines – Speed-Independence–Delay-insensitivity – Classes of Asynchronous Circuits –Delay models – Asynchronous Design Methodologies and Building Blocks–Completion Indicators – Synchronizers – Arbiters– Delay Insensitive Codes–Globally Asynchronous Locally Synchronous (GALS) Designs– Synthesis of Asynchronous Control Logic.

Outcomes:

CO1 Understand advanced topics in digital logic design.

CO2 Understand modelling and verification with hardware description languages.

CO3 Design state machines and data path controllers.

TEXT BOOKS / REFERENCES:

1. Michael D. Ciletti,*Advanced Digital Design with Verilog HDL*, Second Edition, Pearson Higher Education, 2011.
2. Morris Mano and Michael D. Ciletti,*Digital Design: With an Introduction to the Verilog HDL*, Fifth Edition, Pearson Higher Education, 2013.

3. Peter Minns and LanElliott,*FSMBased Digital Design Using Verilog* HDL, Fifth Edition, John Wiley and Sons Ltd, 2008.
4. Parag K. Lala*, Principles of Modern Digital Design,* Second Edition, John Wiley and Sons Ltd., 2007.

18VL613 ANALOG IC DESIGN 3-0-2-4

Objectives:

- To provide exposure in using device models, biasing circuits, small-signal operations, high frequency performance analysis and op amp design concepts.
- To use circuit simulators in the design of electronic circuits based on active devices (particularly MOS device)anddetermination of circuit parameters.

Key words: MOS, SPICE Models, MOS Amplifier, Frequency Compensation.

Contents:

MOS Large-signal and Small-signal–High-frequencyModeling– Short-Channel–Sub-threshold Operation –Leakage Current – MOS Diodes – Active Resistors – Capacitors.

Current Sink and Source–Cascade and CurrentMirrorsConfigurations–Gain-boosting– Current and Voltage references–MOS Inverters – Active Load – Current Source – Push-Pull – Frequency Response.

Single-stage MOS Amplifiers –Miller Effect–High-frequencyEffects–MOSSmall-signalModel of Amplifiers–DifferentialAmplifiers–Active Loaded DifferentialPair–FeedbackAmplifiers–Negative Feedback – Dynamic Response – Inverting and Non-Inverting Amplifiers–LoopGain–Two-Stage CMOSOp-amp – Performance Study of GainandFrequencyResponse –Compensation– Comparators.

Lab:DC– I-V– C-V and $g_m$of MOSFET –S-parameter Simulation Using SPICE/BSIM-4 models – Current Mirrors–Amplifier Topologies with Active Load–Differential AmplifierConfigurations.

Outcomes:

CO1 To make expertise in SPICE based circuit simulators.
CO2 Ability to design active loaded (IC), MOS based single/multi-stage, operational amplifier considering terminal impedance matching.

TEXT BOOKS / REFERENCES:

1. B.Razavi,*DesignofAnalogCMOSIntegratedCircuits*,TataMcGraw-Hill,2002,(Reprint 2015).
2. P.E.AllenandD.R.Holberg,*CMOSAnalogCircuitDesign*,ThirdEdition,OxfordPress, 2011.
3. P.R.Gray,P.J.Hurst,S.H.LevisandR.G.Meyer,*AnalysisandDesignofAnalogIntegratedCircuits*,J ohnWileyandSons Inc., 2009.
4. T.C.Carusone,D.A.JohnsandK.W.Martin,*AnalogIntegrated Circuit Design*,Second Edition, John WileyInc,2012.

18VL631 VLSI DESIGN LABORATORY-I 0-0-4-2

Objectives:

- To Build basic designs and incorporate them into system level design.
- To do experiments using FPGA and other tools for various digital designs.

Keywords: Timing Diagrams, Synthesis Aspects, FPGA and ASIC Libraries, VLSI Tools, Simulation,Synthesis.

Contents:

- Design an adder and 4-bit full adder. Instantiate four 4-bit adders to add two16 bit values, implement in FPGA using switches as input and LED as the output. Refer synthesis report regarding the area, power and speed.
- Using a simulator(SPICE/CADENCE/Synopsis) build a Fulladder schematic using built-in gates.
- Build standard libraries(Inverter, NAND, NOR and AOI) for a given technology using CADENCE/Synopsis. Do DRC, LVS and Extraction.
- Develop the behavioural style HDL code for D-Flip Flop using gated, positive edge andnegative edge clock modes.
- Develop the behavioural style HDL code for 4-bit counter.Develop the structural style HDL code for 4-bit counter using T Flip Flop (use of generate statement, area-performance analysis after synthesize). Compile, synthesize and simulate each design entity and verify the functionality by creatingvector waveform file.
- Design a traffic light controller for an intersection with a main street, a side street, and a pedestrian crossing or a Vending Machine(Implement it on FPGA)
- Using the NAND and NOR standard cells designed in Exp 3, draw the layout for D and SR latch. Do DRC, LVS and Extraction.
- Implement a 4-bit ALU.

Outcomes:

CO1 Ability to implement the designs using front end design environment using top down and bottom up approach.

CO2 Ability to verify the functionalities of the designs.

CO3 Ability to analyse the area, delay trade-offs and performance metrics associated with simulation and synthesis.

TEXT BOOK/REFERENCE:

Lab manuals and online manuals for tools usage and languagereferencemanuals of HDLs.

18VL614 DESIGN VERIFICATION 3-0-0-3

Objectives:

- To introduce verification of hardware designs.
- To provide a practical approach for verification of designs.
- Togive an introduction to FPGA based verification and Emulation of VLSI systems.

Keywords: Verification, Randomization, Direct Programming Interface, Assertions Based Verification, OVM & UVM.

Contents:

Introduction to Verification– Need for Functional Verification –Validation andEmulation– ASIC Verification Concepts– Bottle NeckProblem in ASIC DesignChallenges– Design – FPGA and Emulation based Validation and Testing –MajorVerification Tasks – Creating Verification Plan – LinearTest Bench – Linear Random Test Bench– Self Checking Test Benches – Test Coverage.

Formal Verification–Decision Diagrams – Equivalence Checking –SystemVerilog for Design– Standard Data Types and Literals –Procedures and Procedural Statements –Operators– User-Defined Data Types – Hierarchy and Connectivity –Tasks and Functions –Interfaces –SystemVerilog for Verification–Verification Blocks –Transaction– Level Modeling– SystemVerilog Classes – Random Stimulus – Class-Based Randomization – Functional – Coverage – Queues and Dynamic Arrays– Interprocess Synchronization – Direct Programming Interface (DPI).

SystemVerilog Assertions– Assertion-Based Verification (ABV) – Immediate and Concurrent Assertions – Simple Boolean Assertions – Sequences –Sequence Composition – Advanced SVA Features – Coding Guidelines– Functional Coverage -Practical SVA Application – Introduction to Static Formal Verification–OVM/UVM Verification Componentsand Objects – OVM/UVM Transactions –OVM/UVM Factory Basics.

Outcomes:

CO1 Ability to familiarize verification process and its different methodologies.
CO2 Ability to write test-benches using system verilog in an efficient way.
CO3 Ability to develop algorithms which can automate the design verification process.

TEXT BOOKS / REFERENCES:

1. Chris Spear, *SystemVerilog for Verification: A Guide to Learning the TestBenchLanguage Features*, Third Edition, Springer, 2012.
2. Douglas Perry, andHarry Foster, *Formal Verification: For Digital Circuit Design*, First Edition, McGraw-Hill Education, 2005.
3. S Halsoun and T Sasao, *Logic Synthesis and verification*, Kluwer Academic publishers, 2002.
4. PallabDasgupta, *ARoadMap for Formal Property Verification*, Springer 2006.

18VL615 VLSI SIGNAL PROCESSING 3-0-0-3

Objectives:

- To introduce concepts in the design and implementation of DSP architectures.
- To realize architectures with high throughput, less area and less power.

Keywords: FIR Filter, IIR Filter, Pipelining, Parallel Processing, Folding, Retiming, Systolic.

Contents:

Introduction to Digital Signal Processing Systems – Iteration Bound – Pipelining and Parallel Processing – Retiming.

Unfolding – Folding – Systolic Architecture Design – Pipelined and Parallel Recursive and Adaptive Filters–Scaling and Round off Noise –Digital Lattice Filter Structures.

Bit-Level Arithmetic Architectures – Programmable Digital Signal Processors – Computational Accuracy in DSP Implementations – Adaptive Filters–Kalman Filters.

Outcomes:

CO1 Ability to implement basic digital signal processing blocks like FIR and IIR filters. CO2 Ability to optimize the design by employing various algorithms.

TEXT BOOKS/REFERENCES:

1. Keshab K. Parhi, *VLSI Digital Signal Processing Systems, Design and Implementation*, Wiley, 1999.
2. Venkataramani B and Baskar M., *Digital Signal Processors, Architecture, Programming and Applications*, Tata McGraw-Hill, 2002.
3. Avatar Singh and Srinivasan S., *Digital Signal Processing Implementations Using DSP Microprocessors with Examples from TMS320C54X*, Thomson Learning, 2004.
4. Simon Haykin, *Adaptive Filter Theory*, Prentice Hall, 1997.

18VL616 DESIGN FOR TEST AND TESTING 3-0-0-3

Objectives:

- To introduce the concept of VLSI Testing and analyze the potential of ATPG algorithms.
- To design for testability and explore the built-in-test concepts.
- To learn and understand the challenges involved in scan design and test.

Key words: VLSI Testing, Design for Testability, Automatic Test Pattern Generation, Built-in-self-test, Boundary Scan.

Contents:

Testing of VLSI Circuits– Fault Modeling – Equivalence and Dominance - Logic and Fault Simulation –Testability Measures – Combinational Circuit Test Generation – Redundancy Identification.

ATPG for Roth's D-algorithm – PODEM – Sequential Circuit Test Generation – Time Frame Expansion and Implementation – Design for Testability– Scan Architectures and Testing –Pseudo Random Testing.

Testable Combinational Logic Circuit Design – Design of Testable Sequential Circuits–BIST Architectures –Test-Per-Clock – Test-Per-Scan - BIST Systems – Memory BIST –At-speed Testing – Boundary Scan Architecture – JTAG Standards.

Outcomes:

CO1 Improves the knowledge level in the domain of VLSI Design and Test.
CO2 Enhances the creativity to develop new ATPG Algorithms.
CO3 Enables the student to design for testability.

TEXT BOOKS / REFERENCES:

1. Vishwani D. Agrawal and Michael L. Bushnell, *Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits*, Kluwer Academic Publishers, 2000.
2. Parag K. Lala, *An Introduction to Logic Circuit Testing*, Morgan &Claypool Publishers, 2009.
3. LaungTerng Wang, Cheng Wen Wu and Xiaoqing Wen, *VLSI Test Principles and Architectures – Design for Testability,* First Edition, Morgan Kaufmann Publishers, 2006.
4. MironAbramovici, Melvin A. Breuer andArthurD.Friedman, *Digital Systems Testing and Testable Design*, Jaico Publishing House, 2001.

18VL632 VLSI DESIGN LABORATORY-II 0-0-2-1

Objective:

- To use advanced tools to study front end and back end implementations.
- To build custom circuits using analog and digital environments.

Keywords: Area, Delay, Layout, Power, Timing Analysis, Digital, Analog Circuits Simulation and Analysis.

Contents:

- Data Path Circuits–State Machine in Front End for Simulation –Synthesis –Area and Delay Tradeoff–LayoutRepresentation and Circuit Extraction in Backend.
- Analog Circuits and Mixed Signal Circuit Simulation and Analysis.
- Timing and Power Analysis of Standard Combinational and Sequential Circuits.
- Verification examples using System Verilog.

Outcomes:

CO1 Ability to analyze the circuits built in simulation, synthesis, timing and layout environments using VLSI tools from standard EDA companies.

CO2 Ability to interface between front end and backend design flows, Post layout extraction and simulation.

TEXT BOOKS/REFERENCES:

1. Lab Manuals and online manuals for tools usage.
2. Language reference Manuals of HDLs.

18RM600 RESEARCH METHODOLOGY 2-0-0-2

Unit I:

Meaning of Research, Types of Research, Research Process, Problem definition, Objectives of Research,Research Questions, Research design, Approaches to Research, Quantitative vs. Qualitative Approach,Understanding Theory, Building and Validating Theoretical Models, Exploratory vs. ConfirmatoryResearch, Experimental vs Theoretical Research, Importance of reasoning in research.

Unit II:

Problem Formulation, Understanding Modeling & Simulation, Conducting Literature Review,Referencing, Information Sources, Information Retrieval, Role of libraries in Information Retrieval,Tools for identifying literatures, Indexing and abstracting services, Citation indexes

Unit III:

Experimental Research: Cause effect relationship, Development of Hypothesis, Measurement SystemsAnalysis, Error Propagation, Validity of experiments, Statistical Design of Experiments, FieldExperiments, Data/Variable Types & Classification, Data collection, Numerical and Graphical DataAnalysis: Sampling, Observation, Surveys, Inferential Statistics, and Interpretation of Results

Unit IV:

Preparation of Dissertation and Research Papers, Tables and illustrations, Guidelines for writing the abstract,introduction, methodology, results and discussion, conclusion sections of a manuscript. References,Citation and listing system of documents

Unit V:

Intellectual property rights (IPR) - patents-copyrights-Trademarks-Industrial design geographical indication. Ethics of Research- Scientific Misconduct- Forms of Scientific Misconduct.Plagiarism, Unscientific practices in thesis work, Ethics in science

Outcomes

CO1 Understand and apply some basic concepts of research and its methodologies.
CO2 Able to select and define appropriate research problem and parameters.
CO3 Demonstrate skills to write a research paper.
CO4 Comprehend the ethical practices involved in conducting research and dissemination of results in different forms.

TEXT BOOKS/ REFERENCES:

1. Bordens, K. S. and Abbott, B. B., “Research Design and Methods – A Process Approach”, 8thEdition, McGraw-Hill, 2011
2. C. R. Kothari, “Research Methodology – Methods and Techniques”, 2nd Edition, New Age International Publishers
3. Davis, M., Davis K., and Dunagan M., “Scientific Papers and Presentations”, 3rd Edition, Elsevier Inc.
4. Michael P. Marder,“ Research Methods for Science”, Cambridge University Press, 2011
5. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”.Aspen Law & Business; 6 edition July 2012

18VL798 DISSERTATION 0-0-0-10

Objectives:

- To define the problem of the proposed work.
- To apply the concepts of VLSI design in the selected problem.
- To demonstrate the results of the design concept.

Contents:

Problems and concepts may be defined based on extensive literature survey by standard research articles. Significance of proposed problem and the state-of the art to be explored. VLSI Design tools may be used for demonstrating the results with physical meaning and create necessary research components. Publications in reputed journals and conferences may be considered for authenticating the results.

Outcomes:

CO1 Creation of manpower in the VLSI domain and specialize in the state-of the art technology. CO2 Enable design aptitude and complex problem solving in the VLSI design aspects. CO3 Research publications and filing of patents.

18VL799 DISSERTATION 0-0-0-10

Objectives:

- To define the problem of the proposed work.
- To apply the concepts of VLSI design in the selected problem.
- To demonstrate the results of the design concept.

Contents:

Problems and concepts may be defined based on extensive literature survey by standard research articles. Significance of proposed problem and the state-of the art to be explored. VLSI Design tools may be used for demonstrating the results with physical meaning and create necessary research components. Publications in reputed journals and conferences may be considered for authenticating the results.

Outcomes:

CO1 Creation of manpower in the VLSI domain and specialize in the state-of the art technology.
CO2 Enable design aptitude and complex problem solving in the VLSI design aspects.
CO3 Research publications and filing of patents.

ELECTIVE COURSES

ANALOG CIRCUITS AND DEVICES

18VL701 VLSI SIGNAL CONDITIONING 3-0-0-3

Objectives:

- To make the signal compatible for the next stage by manipulating the signal.
- To introduce Operational Trans-conductance amplifier and OTA based circuits.
- To understand $_{gm/ID}$ based designs and different signal conditioning circuits.

Keywords: OTA, g_m/I_D, Gm-C, NAUTA, Q – tuning, Biquads, Filtering,

Amplification. **Contents:**

Operational Trans-conductance Amplifier basic Considerations – Application Requirements for OTAs used in Filters – The Case for Fully Differential Circuits – Transistor Models – g_m/I_Dbased Design – Single-stage OTAs.

Basic Differential Pair – Telescopic Architecture – Folded Cascode Architecture – Two-stage OTA – Gain Boosting – Common-mode Feedback Implementation– Gm-C Biquad – Trans-conductor Implementation – NAUTA Cell – Source Follower based Filter – Parameter Tuning – Q-tuning – VCF-tuning – Discrete Frequency Tuning / Programming – Tuning Gm over a Wide Range.

Switched Capacitor Filters – Parasitic Sensitive Configurations – Transient and Circuit Analysis – Frequency Response – Aliasing – Periodic AC Analysis – SC Integrators – Martin-SedraBiquad – Low and High Design Q Biquads – Noise Analysis –Precision Analog Circuit Techniques – Applications.

Outcomes:

CO1 Knowledge about $_{gm/ID}$ based design.
CO2 Ability to Understand parameter tuning, filtering and various signal conditioning blocks.

TEXT BOOKS/REFERENCES:

1. Schauman, Rolf and Van Valkenburg, *Design of Analog Filters*, Second Edition, Oxford University Press, 2009.
2. Tony Chan Carusone, David A. Johns and Kenneth W. Martin, *Analog Integrated Circuit Design*, Second Edition, John Wiley Inc., 2012.
3. Gregorian and Temes, *Analog MOS Integrated Circuits for Signal Processing*, Wiley, 1986.

18VL702 SEMICONDUCTOR MEMORY DESIGN 3-0-0-3

Objectives:

- To learn and understand the Memory hierarchy and array structure in the system.
- To learn various types of architecture for semiconductor memories in detail to understand their limitations and improve them.
- To learn and understand the structures and various parameters associated with semiconductor memories.

- To familiarize with cadence and Synopsys in designing memories.
- To understand various aspects of reliability and fault modelling.

Key words: Memory Hierarchy, Memory Array, SRAM, DRAM, Flash Memory, Fault Modeling, Reliability, FRAM, MRAMs.

Contents:

Random Access Memory Technologies – SRAM Cell Structures – MOS SRAM Architecture – MOS SRAM Cell and Circuit Operation – Advanced SRAM Architectures and Technologies – Application Specific SRAMs – CMOS – DRAM – DRAM Cell Theory – Cell Structures – Soft Error Failure in DRAM.

EEPROM Technology – Architecture – Non-volatile SRAM – Flash Memories – Advanced Flash Memory Architecture – RAM Fault Modeling – Volatile and Non- volatile Memory Testing Methods – RAM Fault Modeling – BIST Techniques for Memory – General Reliability Issues – RAM Failure Modes and Mechanism.

Non-volatile Memory Reliability – Reliability Modeling and Failure Rate Prediction – Design for Reliability– Reliability Test Structures – Radiation Effects – Single Event Phenomenon (SEP) – FRAMs – GaAs RAMs – Magneto Resistive RAMs (MRAMs) – Experimental Memory Devices – Memory Hybrids and MCMs (2D) – Memory Stacks and MCMs (3D) – Memory MCM Testing and Reliability Issues – Memory Cards – High Density Memory Packaging.

Outcomes:

CO1 Enable the student to understand the semiconductor memories, their working principle and implementation.

CO2 Able to think innovatively in the related topics.

CO3 Expertise in the area of semiconductor memory to carry out projects/research.

TEXT BOOKS / REFERENCES:

1. Ashok K. Sharma, *Semiconductor Memories: Technology, Testing, and Reliability*, Wiley, 2013.
2. Kevin Zhang,*Embedded Memories for Nano- Scale VLSIs*, Springer, 2009.
3. Santosh K. Kurinec and Krzysztof Iniewski, *Nanoscale Semiconductor Memories: Technology and Applications*, CRC press, 2013.
4. Koichi Ishibashi and Kenichi Osada, *Low Power and Reliable SRAM Memory Cell and Array Design*, Springer, 2011.
5. HaldunHadimioglu, David Kaeli, Jeffrey Kuskin, Ashwini Nanda, JosepTorrellas ,*High Performance Memory Systems*, Springer; 2004 edition.
6. Saraju P. Mohanty and Ashok Srivastava, *Nano-CMOS and Post-CMOS Electronics: Circuits and Design*, Vol 2. , (IET) The institution of Engineering and Technology, 2015.

18VL703 OPTOELECTRONIC DEVICES 3-0-0-3

Objectives:

- To provide students with a view of principles of devices used in optoelectronics industry.
- To make students understand the physics and performance parameters in optoelectronicdevices.
- To make students appreciate design principles by assignments.

Keywords: Optics, Photonics, III-V semiconductor, optical modes, planar devices. **Contents:**

Introduction: Optical Systems and Fundamentals - Basics of Semi-conductor Optics: Elemental and Compound Semiconductors - Electronic and Optical Processes in Semiconductors; P-N Junctions LEDs,Photodetectors and Solar Cells.

Heterostructures, Confinement of Electron Waves, Optical Waveguides and mode theory; Semiconductor Optical Amplifiers (SOA) and Fabry-Perot Lasers - Coupled Mode Theory, DBR and DFB Lasers.

Silicon Photonics: Integrated Optical Passive and Active Components; Tunable Filters, Delay-Lines and Switching Circuits in SOI Platform; CMOS Technology: Electrical vs. Optical Interconnects. Special topic: high speed photonic devices. Mandatory mini-project to be evaluated as internal.

Outcome:

CO1 Students in VLSI should have clarity of their applicability in opto-electronic industry; CO2 Students will gain sufficient background if pursuing a research career.

TEXT BOOKS / REFERENCES:

1. AmnonYariv, *Optical electronics*, Oxford University Press, 1990.
2. William S.C. Chang, Fundamentals *of guided wave optoelectronic devices,*CambridgeUniversity Press, 2009.
3. L. Pavesi, G. Guillot, *Optical interconnects: the silicon approach*, Springer, 2006.
4. C.F. Klingshirn, *SemiconductorOptics*, Springer, 2012.
5. Shun Lien Chuang, *PhysicsofPhotonic devices*, John Wiley and Sons, 2009.
6. Eds. Lukas Chrostowski, Krzysztof Iniewski, *High speed photonics interconnects*,CRC Press, 2017.

18VL704 MIXED SIGNAL VLSI DESIGN 3-0-0-3

Objectives:

- To give an insight in to the design and analysis of data converters, especially SAR ADC.
- To introduce Verilog AMS for modeling various basic blocks.

Contents:

Nyquist Sampling theorem, Sample and Hold Circuits – Top & Bottom Plate Sampling. Integrator-based filters: The gm-C filter. Basic and Clocked Comparators.Basics of PLLs (Phase Locked Loops) Introduction to VerilogA and VerilogAMS.

Ideal ADCs- Quantization Noise and SNR. Non-idealities- Nonlinearity (DNL, INL) and offsets-SFDR- Nyquist ADC architectures- Flash ADC- Successive Approximation Register (SAR) ADC-Pipelined ADC- Design of SAR ADC- Capacitor array DAC- Matching of capacitors-Choice of unit capacitance.

SAR ADC-Split capacitor array-Techniques of improving SNR-Averaging-Introduction to Oversampling Converters-Noise-shaping.Basics of Sigma-Delta ADCs.

Outcomes:

CO1 Familiarization of the working of data converters, especially SAR ADCs.
CO2 Ability to model and verify basic circuits with Verilog-AMS.

TEXTBOOKS / REFERENCES:

1. R. Jacob Baker, *CMOS Mixed Signal Circuit Design*, Wiley India Pvt. Ltd, 2008.
2. R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*, Third Edition, IEEE Press, 2010.
3. David A. Johns and Ken Martin, *Analog Integrated Circuit Design*, Wiley India Pvt.Ltd, 2008.
4. Kenneth S. Kundart and Olaf Zinke, *The Designer's Guide to Verilog- AMS*, Springer, 2004.

TESTING AND VERIFICATION

18VL711 VLSI HARDWARE SECURITY AND TRUST 3-0-0-3

Objectives:

- To explore the various security threats in ICs.
- To know various countermeasures to address security threats.

Keywords: Trojan Attacks, Detection and Isolation, Side-channel Attacks, Physically Unclonable Functions, Trusted Platform Modules.

Contents:

Integrated Circuits (IC) Trojans – Vulnerabilities in Combinational and Sequential Logic – Finite State Machines – Trojan Attacks – Detection and Isolation – Side-channel Attacks include Power Spectrum Analysis.

EM Analysis – Timing Analysis – Fault Injection- FPGA Security Attacks - Physical Attacks on FPGA – Physical Design Layers – Emerging Hardware Security and Trust – Trusted Platform Modules (TPM) for Hardware – Physically Unclonable Functions (PUFs) .

True Random Number Generators (TRNG) – RFID Tag-Hardware System Tampering – Tamper Resistant Hardware Design Techniques – Anti-Counterfeiting for Microelectronics Devices – Protection of Intellectual Property (IP) –IC Reverse Engineering –Reverse Engineering counter measures.

Outcomes:

CO1 Ability to understand effects of hardware trojans.
CO2 Ability to understand the difficulties in detecting and identifying security threats.
CO3 Ability to understand various techniques for trusted designs.

TEXT BOOKS/REFERENCES:

1. M. Tehranipoor and C. Wang, *Introduction to Hardware Security and Trust,* Springer, 2011.
2. J. Plusquellic, *Trojan Taxonomy*, University of New Mexico, http://www.ece.unm.edu/~jimp/HOST.
3. 3.D. Agrawal, S. Baktir, D. Karakoyunlu, P. Rohatgi and B. Sunar, *Trojan Detection using IC Fingerprinting,* IEEE, Symposium on Security and Privacy, 2007.

4. G. Edward Suh and S. Devadas,*PhysicalUnclonable Functions for Device Authentication and Secret Key Generation*, DAC-2007.

18VL712 STATIC TIMING ANALYSIS 3-0-0-3

Objectives:

- To learn basic concepts of static timing analysis and apply them to constrain a design.
- Apply these concepts to set constraints, calculate slack values for different path types, identify timing problems.
- Analyze reports generated by static timing analysis tools.

Keywords: Timing Analysis Concepts, Timing Exceptions, Timing Violations, Noise-crosstalk glitch.

Contents:

Static Timing Analysis Concepts – Timing Exceptions– Timing Violations – Capacitance and Transition Violations – Various Timing Paths – Constraining Paths – Interconnect Parasitics-Path Delay Calculation –Cell Delay – Net Delay – Delay Calculation with Interconnect – Slew Merging – Slack Calculation.

Crosstalk and Noise–crosstalk Glitch Analysis–Crosstalk Delay Analysis Setup and Hold Analysis – Timing Verification–Synchronization – Synchronization Failure – Probability of Entering a Meta Stable State – Probability of Staying in the Meta stable State–Multi-cycle Paths–False Paths–Timing Across Clock Domains– Clock Network Optimization –Clock Skew– Scheduling.

Clock Distribution Problem– Off-Chip Clock Distribution – Clock Trimming – On-Chip Clock Distribution– On-Chip Clock Tree – Reducing Jitter– Pre-Layout Clock Specification – Post-Layout Clock Specification –Parallel Timing Optimization –Circuit Partitioning for Independent Timing Regions – Post-Silicon Timing Validation–Post-Silicon Tuning – on-chip Variations –Time Borrowing–Clock Gating Checks – sign-off Methodology–Statistical Static Timing Analysis.

Outcomes:

CO1 Ability to identify and apply timing arc information from a library.
CO2 Ability to use wire-load information to calculate net delays.
CO3 Ability to identify the properties of a clock, including period, edges, slew, and duty cycle.
CO4 Ability to apply setup and hold checks to diagnose design violations.

TEXT BOOKS / REFERENCES:

1. J. Bhasker, R.Chadha, *Static Timing Analysis for Nanometer Designs: A Practical Approach*, Springer, 2009.
2. William J. Dally and John W. Poulton, *Digital Systems Engineering* Cambridge University Press, 2008.
3. Charles J. Alpert Dinesh P. Mehta Sachin S. Sapatnekar, *Handbook ofAlgorithms for Physical Design Automation*, CRC Press, 2009
4. HimanshuBhatnagar, *Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time*, Second Edition,Kluwer Academic Publishers, 2002.

18VL713 DESIGN FOR MANUFACTURABILITY 3-0-0-3

Objectives:

- To introduce basic concepts of industrial and large scale manufacturing process for Silicon industry.
- Graduate students to develop an understanding of considering manufacturability as a requirement of design itself and tailor their designs accordingly.

Keywords: Industrial DFM, product level DFM, design level DFM, DFM metrics and DFM

tools. **Contents**:

Introduction to DfM- Three Product Questions, SMART Goals and Is/Is Not- Migrating Industrial DfM into IC Manufacturing The Rule of 10-Concurrent Engineering-Doing it Right the First Time.

Product Level DfM- Product Definition, Product architecture, System on Chip vs. System in Package; Design Level DfM.

Logical Synthesis- Electrical Models- MOSFETs- Circuits- DfM Metrics-Yield (DfY)- Testability (DfT)-Mask Ratio-Cycle time-DfM Tools-Design Rule Check Engines-IP Management.

Outcomes:

CO1 Ability to identify and apply timing arc information from a library.
CO2 Ability to use wire-load information to calculate net delays.
CO3 Ability to identify the properties of a clock, including period, edges, slew, and duty cycle.
CO4 Ability to apply setup and hold checks to diagnose design violations.

TEXT BOOKS / REFERENCES:

1. ArturBalasinski,*Semiconductors:Integrated Circuit Design for Manufacturability,* by CRC Press,2017.
2. Anupama B. KauL,*Microelectronics to Nanoelectronics: Materials, Devices & Manufacturability*, CRC Press,2017.
3. James G.Bralla,*Design for Manufacturability Handbook,* ISBN: 9780070071391 Second Edition, McGraw-Hill Companies, Inc., 1999.

18VL714 FORMAL VERIFICATION 3-0-0-3

Objectives:

- Learn about formal modeling and specification languages.
- Learn about main approaches in formal VLSI design verification.

Contents:

Introduction to Formal verification- Challenges- Equivalence Checking CNF formulas – SAT - Stable set of points – Testing Satisfiability. Mixed BDD and SAT techniques - SAT solvers- BDD – Model checking – Comparing SAT & BDD approach- Affinities – Recursion Tree –Decision diagram – ZBDDs.

Symbolic DLL – Breadth first SAT - Decision Diagram Pre-processing and Circuit Based SAT - BED Pre-Processing – Circuit based SAT – BDD sweeping and SAT – Reachability-Reachability Analysis – BDDs at SAT leaves – SAT Based Symbolic Image and Pre Image - Equivalence Checking of Arithmetic Circuits.

Functional Properties – Decompositions - BMDs - Bit Level Verification – Extracting – Framework - Property Checking - Verification Environment – Exploiting Symmetries – Automated Data Path Scaling – Property Checking cases –Assertion based Verification.

Outcomes:

- Use automated and interactive tools to validate models and design.
- To be able to write and understand formal requirement specifications.

TEXT BOOKS/REFERENCES:

1. Lam, William K. *Hardware Design Verification: Simulation and Formal Method-Based Approaches,* Prentice Hall Modern Semiconductor Design Series. Prentice Hall PTR, 2005.
2. Fujita Masahiro, IndradeepGhosh and Mukul Prasad. *Verification techniques for system- level design*. Morgan Kaufmann, 2010.
3. Rolf Drechsler,*Advanced Formal Verification,* Kluwer Academic Publication,2004.
4. Douglas L Perry Harry D Foster, *Applied Formal Verification*, McGraw Hill, 2005.

COMPUTATIONAL VLSI

18VL721 COMPUTER AIDED DESIGN OF VLSI CIRCUITS 3-0-0-3

Objectives:

- To learn the VLSI Design methodologies.
- To understand the VLSI design automation tools.
- To understand placement, floor planning and routing and synthesis.

Contents:

Introduction to VLSI Design methodologies- Basics of VLSI design automation tools-Data structures for the representation of graphs-computational complexity-Graph algorithms-Combinatorial optimization problems-Decision problems - complexity classes - NP-completeness and NP-hardness-unit size placement problem- Back tracking and Branch-and-Bound.

Placement algorithms- Partitioning-Kernighan-Lin partitioning algorithm-Terminology and floor plan representation-optimization problems in floor planning-types of local routing problems-area routing-channel routing-global routing and its algorithms-classification of compaction algorithms-1 D compaction-2D compaction.

Combinational Logic Synthesis- Binary Decision Diagrams-hardware models for high level synthesis-Allocation-Assignment and scheduling- scheduling algorithms.

Outcome:

CO1 Ability to apply the algorithms for understanding the physical design flow.

TEXTBOOKS/REFERENCES:

1. S.H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley & Sons, 2002.
2. N.A. Sherwani, *Algorithms for VLSI Physical Design Automation*, Kluwer Academic Publishers, 2002.
3. Sadiq M. Sait, Habib Youssef, *VLSI Physical Design automation: Theory and Practice*, World Scientific 1999.

18VL722 PHYSICAL DESIGN OF INTEGRATED CIRCUITS 3-0-0-3

Objectives:

- To develop algorithms for placement and power routing.
- To analyze the setup and hold times in physical domain.
- To decrease the timing cost by adopting new routing techniques.

Keywords: Placement, Timing Analysis, Power Planning, Multivoltage, Clock Tree Synthesis, Routing,RC Extraction.

Contents:

Physical IC Design–Objectives–VLSI Physical Design Cycle–Circuit Layout–Partitioning–Floor Planning–Placement–Specific Floor Planning Problems–Power Density Map–Advanced Low-Power Floor Planning–Multi-Voltage PG Routing–Floor Planning for Low Power.

Timing Analysis &Optimization–Basic Timing Checks–Timing Constraints(SDC) – Timing Corners– Timing Report Analysis–Crosstalk and Noise –Clock Distribution Networks–Clock Tree Synthesis– Clock Skew–Clock Power– Area-Congestion Map–Clock Tree Optimization–High Fan-Out Synthesis (HFS)–Routing Steps in Physical Synthesis.

Classification of Routing Methods–Grid-Based Routing System–Global Routing–Top-Level Congestion–Detailed Routing–Channel Routing Problem–Analysis and Optimization Types–Best/Worst Analysis –Combination of Corners and Modes–Parasitic Extraction (RC Extraction)–Chip Finishing Overview–Antenna Fixing–Parasitic (SPEF or SBPF)–Final Validation– Net List Output– GDS2 Output–Basic FPGA Architecture–Technology Mapping for FPGA - FPGA Routing Algorithm.

Outcomes:

CO1 Familiarize with the latest techniques adopted in physical domain.
CO2 Familiarize with the concepts of timing violation and fixing.

TEXT BOOKS/REFERENCES:

1. Andrew B. Kahng, Jens Lienig, Igor L. Markov,*From Graph Partitioning to Timing Closure,*Jin Hu, Springer 2011.
2. K. Golshan, *Physical Design Essentials: An ASIC Design Implementation Perspective*, Springer, 2010.
3. J.P. Uyemura, *Modern VLSI Design – System-on-Chip Design*, Prentice-Hall, 2002.
4. A. B. Kahng,*VLSI Physical Design: From Graph Partitioning to Timing Closure*, Springer, 2011.

5. Stephen D. Brown, Robert J. Francis, Jonathan Rose andZvonko G. Vranesic, *Field-Programmable Gate Arrays*, Springer, 2012.

18VL723 EMERGING ARCHITECTURES FOR MACHINE LEARNING 3-0-0-3

Objectives:

- To introduce new paradigms in computing.
- To get an exposure to popular Cloud and IoT technologies.
- To introduce the potential of FPGAs in neural networks and bioinformatics.
- Provide hands on exposure in designing systems using state of the art computing tools.

Keywords: GPU, CUDA, Cloud and IoT, Machine Learning.

Contents:

Accelerated Computing – GPUs – Overview of GPU Architectures – CUDA – OpenCL – Case Studies IoT and Cloud Architectures – Use Cases – VLSI Design Challenges for IoT– Power – Area and Security – Intel Dashboard Framework.

Overview of Cloud Computing – Introduction to Hadoop Framework – Case Study – FPGA Architectures for Neural Networks and Bioinformatics – Review of Neural Networks.

Data Precision and Implementation Issues – Case Studies of Regression Implementation – FPGA and Reconfigurable Architectures for Bioinformatics – Database Search – Sequencing and Alignment.

Outcomes:

CO1 Ability to design neural network and high performance bioinformatic database analysis systems.
CO2 Ability to design solution for solving problems in a Big Data Cloud Environment.
CO3 Ability to suggest GPU based solutions for dataflow intensive problems.
CO4 Ability to use IoT technologies to design efficient applications.

TEXT BOOKS / REFERENCES:

1. David B. Kirk, Wen-Mei W. Hwu, *Programming Massively Parallel Processors: A Hands-on Approach*, Second Edition, Morgan Kauffman, 2016.
2. Bertil Schmidt, *Bioinformatics: High Performance Parallel Computer Architectures*, CRC Press, 2011.
3. Amos R Omondi and Jagath C Rajapakse*, FPGA Implementation of Neural Networks,* Springer 2006.
4. ArshdeepBahga and Vijay Madisetti, *Internet of Things A Hands on Approach*, Published by the Authors, 2014.
5. Bishop, Christopher M. *Machine learning and pattern recognition*, Information Science and Statistics. Springer, Heidelberg, 2006.

18VL724 WAVELETS AND APPLICATIONS 3-0-0-3

Objectives:

- To study the analysis, design and applications of filter banks and wavelets.
- To get hands-on Experience with Software.

Keywords: CWT, DWT, Legendre Polynomials, Multi Wavelets, EZW.

Contents:

Introduction to wavelets-Vector Space-Functions and function spaces- Continuous time Fourier Transforms-Short time Fourier transforms-The uncertainty principle and time-frequency tiling-Discrete wavelet transforms-Scaling and Wavelet Functions – Filter Banks.

Legendre Polynomials – Recurrence Formula – Laplace's Integral Formula – Design of Orthogonal Wavelet Systems – Bi-orthogonal Wavelet – Introduction to Lifting Scheme – Dealing with Signal Boundaries – Multi Wavelet – Frequency Domain Approach – Design of Wavelet.

Wavelet in Image Processing – Biomedical Applications – Data Compression – EZW Algorithm – De-noising – Edge Detection – Object Isolation – Audio Coding – Communication Applications – Channel Coding – Speckle Removal – Image Fusion–Filter Design – Signal Analysis – Image Compression– PDEs –Wavelet Transforms on Complex Geometrical Shapes.

Outcomes:

CO1 Ability to use wavelets for non stationary signals.

CO2 Ability to use wavelets for various applications including wave propagation, data compression, signal processing, image processing, pattern recognition and computer graphics.

TEXT BOOKS/REFERENCES:

1. SomanK. P. andRamachandran K. I., *Insight into Wavelets from Theory to Practice*, Prentice Hall, 2004.
2. Rao R. M. and Ajith S. Bopardikar, *Wavelet Transforms - Introduction to Theory and Applications*, Pearson Education, 1999.
3. Howard L. Resnikoff and Raymond O. Wells, *Wavelets Analysis the Scalable Structure of Information*, Springer, 1998.
4. Strang G. and Nguyen T. Q., *Wavelets and Filter Banks*, Wellesley Cambridge Press, 1998.

ARCHITECTURE

18VL731 VLSI ARCHITECTURES FOR MULTICORE AND HETEROGENEOUSCOMPUTING 3-0-0-3

Objectives:

- To understand the performance of multi-core processors and high-performancecomputing systems.
- To understand the architectural considerations and VLSI implementation details.
- To introduce advance computer architectural techniques.

Key words: Parallelism, Scheduling, Power, Energy.

Contents:

Review of Types of Parallelism –Instruction Level Parallelism –Thread Level Parallelism –Limits of ILP–Parallel Processing Architectures –Superscalar–VLIW–Scheduling Techniques–Static and Dynamic Schemes.

Inter-Processor Communication Schemes –Bus-Based– Shared Memory– Distributed Memory and Network on Chips –Performance Analysis–Understanding the Impact of the Architectural Modifications on Execution Time on Diverse Applications.

Introduction to Markovian/Stochastic Models for Heterogeneous Computing–Operating System - Role of Multi-Cores –Case Study for Heterogeneous Architectures.

Outcome:

CO1 Ability to analyze performance using state-of-the art simulator for multi-core architectures.

TEXT BOOKS/REFERENCES:

1. Hennesey and Patterson, *Computer Architecture*: *A QuantitativeApproach,*FifthEdition,Morgan Kaufmann, 2012.
2. K. Uchiyama, F. Arakawa, H. Kasahara, T. Nojiri, H. Noda, Y. Tawara, A. Idehara, K. Iwata and H. Shikano, *Heterogeneous Multi-core Processor Technologies for Embedded Systems*, Springer, 2012.
3. J. Dongarra and A.L. Lastovetsky, *High Performance Heterogeneous Computing*, Wiley Series, 2009.
4. Abderazek Ben Abdallah, *Advanced Multicore Systems-On-Chip: Architecture, On-Chip Network, Design*, Springer 2017.

18VL732 HARDWARE SOFTWARE CO-DESIGN 3-0-0-3

Objectives:

- To introduce the design of mixed hardware-software systems.
- To partition simple software programs into hardware and software components.
- To identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components.

Keywords: Co-Design Models, SystemC, Scheduling, Co-Simulation.

Contents:

Introduction To System Level Design –Generic Co-Design Methodology–Hardware-Software Co-Design Models and Architectures –Language for System Level Specification Design and Modeling (SpecC, ArchC And SystemC).

Design Representation for System Level Synthesis –Models of Computation–Architectural Selection–Partitioning–Scheduling and Communication.

Hardware - Software Co-Simulation–Synthesis–Verification and Virtual Prototyping Implementation Case Studies – Performance Analysis and Optimization – Re-Targetable Code Generation – FPGAS.

Outcomes:

CO1 Ability to analyze hardware-software co-design problems for systems with moderate complexity.
CO2 Apply hardware-software co-design methods and techniques to practical problems.
CO3 Applying different levels of abstractions and provide models for verification of the architecture and functionality for embedded co-design solutions.

TEXT BOOKS / REFERENCES:

1. Patrick R. Schaumont,*A Practical Introduction to Hardware/Software Co-design,* Second Edition, Springer, 2013.
2. Jorgen Staunstrup and Wayne Wolf,*Hardware/Software Co-design: Principle and Practice,* Kluwer Academic Publishers, 1997.
3. Giovanni De Micheli*, Readings in Hardware Software Co-design*, Morgan Kaufmann, Academic Press, 2002.
4. Sao-Jie Chen, Kuang-Huei Lin, Pao-Ann Hsiung and Yu-Hen Hu*, Hardware Software Co-Design of a Multimedia SOC Platform*, Springer, 2010.
5. *Vivado Design Suite User Guide: Embedded Processor Hardware Design* UG898 (v2017.3) October 27, 2017.

18VL733 RECONFIGURABLE COMPUTING 3-0-0-3

Objectives:

- To introduce architecture that enables high performance computation as well as the supporting application mapping process.
- To familiarize wide range of reconfigurable architectures.
- To explore different opportunities for the use of reconfigurable architectures.

Key words: FPGA, Reconfiguration, high-level synthesis.

Contents:

Reconfigurable Computing Hardware –Survey of FPGA and non-FPGA devices – Fine-grained – Coarse-grained - Reconfiguration Management – Partial and Dynamic ReconfigurationProgramming.

Reconfigurable Computing Systems–Mapping Applications to Reconfigurable Systems –High-level Synthesis–Area-Performance – Power-aware Mapping.

Placement – Layout and Routing–Application Development–Case study with Applications and Solutions from Different Domains.

Outcomes:

CO1 Ability to understand the fundamentals of FPGA and non-FPGA reconfigurable architectures and design.
CO2 Explore to the state-of-the-art tools in reconfigurable computing.

TEXTBOOKS / REFERENCES:

1. Scott Hauck and Andre Dehon, *Reconfigurable Computing: The Theory and Practice of FPGA Based Computation*, Elsevier, 2008.
2. Christophe Bobda, *Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications*, Springer 2007.

18VL734 ELECTRONIC SYSTEM LEVEL DESIGN 3-0-0-3

Objectives:

- To learn Electronic System Level Design and Verificaion flow and tools.
- To understand virtual prototyping and its advantages.
- To familiarize SystemC based design and debug.
- To learn the basics of Transaction Level Modelling and High Level Synthesis.
- To familiarize on Accrellera consortium, its activities and standards.

Keywords: Electronic System level design, Architecture Exploration, Open Source Languages,SystemC, ArchC, SpecC, Virtual Platform, Virtual Prototyping, Transaction Level Modelling, High level Synthesis and Accellera.

Contents:

Introduction to Electronic System Level Design– Hybrid Design – ESLD Flows and Methodologies – Architecture Exploration–Hardware-software Partitioning.

Models for ESLDesign– Open Source Languages–SpecC–ArchC and SystemC for ESLD– Transaction Level Modelling Building Platform Models in SystemC.

High Level Synthesis– ESL Verification – Virtual Platform and Virtual Prototyping– Debugging SystemC Platform Models –SystemCBasedPowerEvaluation –SystemCStandards and AccelleraInitiatives ESLD – Project Based Practice design.

Outcomes:

CO1 Basic knowledge of Electronic System level Design and Verification.
CO2 Ability to design and verify systems using SystemC.

TEXT BOOKS / REFERENCES:

1. SandroRigo, Rodolfo Azevedo and Luizsantos, *Electronic System Level Design – An Open Source Approach*, Springer, 2011.
2. Brian Bailey and Grant Martin, *ESL Models and their Application in Electronic System Level Design and Verification in Practice*, Springer, 2010.
3. Daniel Grobe and Rolf Drechsler*, Quality Driven SystemC Design,* Springer, 2010.
4. Mark Burton and Adam Morawiec, *Platform Based Design at Electronic System Level – Industry Perspectives and Experience*s, Springer, 2006.

18VL735 LOW POWER VLSI CIRCUITS 3-0-0-3

Objectives:

- To provide a comprehensive idea about different sources of power dissipation in VLSI circuits.
- To introduce power estimation methods.
- To understand different power optimization methods and challenges.
- To learn to apply low power techniques at all levels of design cycle and also during operation.

Keywords: Static power, switching power, short circuit power, probability, low power designs, Pareto Optimization, Dynamic Voltage Scaling, Dynamic Frequency Scaling, Power and clock gating.

Contents:

Importance of Low Power Consumption – Design for Low Power – Deep Submicron and Nanometer MOS Transistors and Models – Sources of Static and Dynamic Power Consumption in MOS Devices – New Device Technologies for Reducing Leakage Current – Basics of Power and Energy.

Power Optimization during Design Cycle – Architecture – Algorithm and System Levels – Power Optimization of Interconnects and Clocks – Dynamic Voltage Scaling – Clock Distribution – RTL power estimation and optimization – Model granularity – Model parameters – Model semantics – Model storage and Model construction.

Power Optimization in Memories – Power in Cell Arrays – Power for Read and Write Accesses – Low Power Memory Technologies – Standby Power Optimization of Circuits and Systems – Power Optimization of Circuits and Systems during Operation – Low Power Design Methodologies and Flows – Power Characterization and Modeling – Low Power Clock – Data and Power Gating – Power Integrity.

Outcomes:

CO1 Understanding about various sources of power dissipation.
CO2 Ability to estimate the power for given circuits.
CO3 Ability to design low power digital VLSI circuits.

TEXT BOOKS / REFERENCES:

1. Jan M. Rabaey, *Low Power Design Essentials*, Springer, 2009.
2. Christian Piguet, *Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools*, CRC Press, Taylor and Francis, 2006.
3. RakeshChadha and J. Bhaskar, *An ASIC Low Power Primer, Analysis, Techniques and Specification*, Springer,2013.
4. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons and Kaijian Shi, *Low power Methodology Manualfor System on Chip*,Springer, 2007.

18VL736 NETWORK ON CHIP 3-0-0-3

Objectives:

- To understand why there is a need for NoC in SoC.

- To understand and analyze the various types of NoC architecture available and its use in present day applications.
- To learn and understand about the various noise sources affecting the interconnection links and the design of low power interconnection link.
- To understand the working of various components used in NoC.
- To learn and understand the different types of switching, routing, addressing techniques and methods available for controlling the congestion and control flow in NoC.

Keywords: System on Chip(SoC), Network on Chip(NoC), Architecture, Topology, Signalling, Traffic patterns, Routers, Interconnection links, Switching, Routing, Addressing, Congestion control, Flow control, Network Interface.

Contents:

Introduction to NoC– SoC objectives and NoC needs – OSI Layer Roles in NoC– Topology Exploration – Traffic Modeling – Physical Layer – Interconnection in DSM SoC– High Performance Signaling.

Building blocks of NoC– Data Link Layer - On Chip Communication Reliability – Network and Transport Layer - Router Design – Switching Technique – Addressing and Routing Techniques – Congestion Control and Flow Control.

NoC Based System Integration – NOC Interface Design and Clock Distribution – Case Study on NoC Architecture for Mobile Application.

Outcomes:

CO1 Ability to understand the need for NoC and the design anNoC architecture.
CO2 Ability to select a suitable traffic pattern for the analysis of the architecture depending upon the traffic load of a given application.
CO3 Ability to select a suitable switching and routing techniques for the transmission of information from one node to another node satisfying the performance needs.
CO4 Ability to handle the congestion and flow control problems, which generally arises in anNoC architecture.

TEXT BOOKS / REFERENCES:

1. Dally, William James, and Brian Patrick Towles. *Principles and practices of interconnection networks*. Elsevier, 2004.
2. KonstantinosTatas, Kostas Siozios, DimitriosSoudris, Axel Jantsch, *Designing 2D and 3D Network on Chip Architecture*, Springer, 2013.
3. Glovanni De Micheliand Luca Benini, *Network on Chip: Technology & tools*, Morgan Kaufmann Publisher, 2006.
4. Axel Jantsch and HannuTenhunen, *Network on chip*, Kluwer Academy, 2003.
5. NicopoulosChrysostomos and Narayanan, *Network on Chip Architecture: A Holistic Design Exploration*, *Lecture Notes in Electrical Engineering*, Springer, 2009.

CYBERPHYSICAL SYSTEMS

18VL741 EMBEDDED SYSTEM DESIGN 3-0-0-3

Objectives:

- To learn the architecture of ARM Cortex-M Microcontroller for embedded design.
- To practice embedded software programming using KEIL platform.
- To learn and understand various design and implementation of simple embedded systems.

Keywords: Microcontroller, ARM, Embedded Systems, Software Architecture, RTOS, Semaphores, PLL, UART, Timer, ADC, DAC, Interrupts, Device Drivers.

Contents:

Microcontroller Fundamentals – ARM–ASM Programming and basics of C – I/O Interfacing (LED and Switch) – Microcontroller Ports – Design and Development Process Architecture – Micro-architecture – Design – Implementation – Verification and Validation.

Development Tools – Block Diagrams – Flowcharts – Call Graphs – Dataflow Graphs – Finite State Machines – Parallel Interface – GPIO – Serial Interface – UART – PLL Programming – Timer – Fixed Point Software – Structs – Stacks and Recursion using ASM Programming.

Device Driver – Interfacing with a Hitachi HD XXX Display – I/O Synchronization – Interrupts – DAC – Music Synthesis and Music Playback – ADC – Real-world Interfacing and Data Acquisition – Applications using ADC– DAC – Interrupts – UART–Display Device Driver – Memory Management in Embedded Systems – Shared Data Problem – RTOS.

Outcomes:

CO1 Ability to understand any other microcontrollers.
CO2 Ability todesign an optimised system considering both software and hardware aspects.
CO3 Ability to analyse the necessity of a particular hardware.

TEXT BOOKS/REFERENCES:

1. Jonathan Valvano,*Embedded Systems: Introduction to ARM® CortexTM-M Microcontroller*, Volume 1, Fourth Edition, Create Space Independent Publishing Platform, 2012.
2. Arnold S. Berger, *Embedded System Design*, First Edition, CRC Press, 2001, (Reprint 2002).
3. David E. Simon, *An Embedded Software Primer*, First Edition, Pearson Education,2001.
4. Steve Heath,*Embedded Systems Design*, Second Edition, Newnes, 2002.
5. Marilyn Wolf ,"*Principles ofEmbedded Computing System Design*" ISBN:9780128053874, 2016.

18VL742 FPGA BASED SYSTEM DESIGN 3-0-0-3

Objectives:

- To understand FPGA Design Flow at the architectural and system design.
- Acquire a good background in block-based design using standard system level tools.
- Familiarization with embedded system design and debug using soft and hard processors in FPGA.

Key words: System Level Design, FPGA Design, Embedded Design.

Contents:

Review of FPGA Architecture and Design Flow-Introduction to Block Based Design.

Soft and Hard Processors-Single and Multiport Memories-IP Subsystems and IP Integration.

High Level Synthesis Flow-Design of a pipelined processor-Communication Buses-Case Studies. **Outcomes:**

CO1 Understand block based design for building SoC systems on FPGAs.
CO2 Ability to design simple SoCs on FPGA platform by integrating processor, memories, bus controllers and other IP subsystems, verify and implement them.
CO3 Learn how to identify appropriate subsystems for implementing a given design problem.

TEXT BOOKS / REFERENCES:

1. ZainalabedinNavabi,*Embedded Core Design with FPGAs*, First Edition, McGraw Hill, 2008.
2. Wayne Wolf, *FPGABased System Design*, Prentice Hall, 2004.
3. Xilinx Inc, *Vivado Design Suite User Guide.*

18VL743 CRYPTOGRAPHY 3-0-0-3

Objective:

- To study the fundamentals of cryptography

Contents:

Introduction to Probability Theory– Information Theory – Complexity Theory and Number Theory – Private-Key – Cryptosystems – Classical Ciphers – DES Family – Product Ciphers – Lucifer Algorithm – Modern Private Key Cryptographic Algorithms – Differential Cryptanalysis – Linear Cryptanalysis – S-box Theory – Propagation and Nonlinearity – Construction of Balanced Functions.

Public-Key Cryptosystems – RSA Cryptosystem – Merkle-Hellman Cryptosystem – McEliece Cryptosystem – ElGamal Cryptosystem – Elliptic Curve Cryptosystems – Probabilistic Encryption – Pseudo-Randomness – Polynomial Indistinguishability – Pseudorandom Bit Generators – Pseudorandom Function Generators – Super Pseudorandom Permutation Generators – Hashing – Theoretic Constructions – Hashing based on Cryptosystems – MD Family – SHA Family – Keyed Hashing

Digital Signature – Generic Signature Schemes – Rabin Signatures – Lamport Signatures – Matyas-Meyer Signatures – RSA Signatures – Elgamal Signatures – Blind Signatures – Undeniable Signatures – Fail-Stop Signatures – Time Stamping – Secret Sharing – Threshold Secret Sharing (*T*, *T*) –Threshold Schemes – Shamir Scheme – Blakley Scheme – Modular Scheme – General Secret Sharing – Stream Ciphers – Linear Complexity – Berlekamp-Massey Algorithm – Non Linear Feedback Shift Registers.

Outcome:

CO1 Application of the concepts of cryptography

TEXT BOOKS / REFERENCES:

1. Josef Pieprzyk, Thomas Hardjono and Jennifer Seberry*, Fundamentals of Computer Security,* Springer, 2003.

2. Alfred J. Menezes, Paul C. Van Oorschot and Scott A. Vanstone*, Handbook of Applied Cryptography,* CRC Press, 1996.
3. Abhijith Das and VeniMadhavanC. E.*, Public-key Cryptography, Theory and Practice,* Pearson Education, 2009.

RF INTEGRATED CIRCUITS

18VL751 CMOS RFIC DESIGN 3-0-0-3

Objectives:

- To learn the design of CMOS RF IC needed to build Transceiver (Transmitter and Receiver) for mobile/satellite/defense communication.
- To get hands-on training of designing of RF/Analog IC Design in Lab.

Keywords: Small Signal Model, Noise Analysis, Low Noise Amplifier, Broadband Amplifier, RF Oscillators, Mixers, Power Amplifiers.

Contents:

Small Signal RF Model of MOSFET – Noise in MOSFET and in Circuit – Non-linearity – 1-dB Gain Compression Point – InterModulation and IIP3/OIP3 – Dynamic Range – Sensitivity –RF Transmitter and Receiver Architectures with Hartley Architecture of Receiver – Impedance Matching.

RF Low Noise Amplifier – Design of Common Source – Common Gate –Cascode and Differential Configurations with Implementations by Inductors –Microstrip and CPW Transmission Lines – Broadband Monolithic Distributed Amplifier with CPW Inductive Transmission Lines – RF Oscillators –Ring Oscillator – LC Cross-Coupled/negative-resistance Oscillator – Distributed Oscillator and Voltage Controlled Oscillator (VCO) – Use of MOSFET as MOS-Varactors in VCO, Quadrature VCO – Phase Noise in Oscillators.

RF Mixers – Active Down-conversion Mixers such as Single-Balanced – Double-Balanced/Gilbert Cell Mixers – Phase lock Loop (PLL) – Phase Frequency Detector (PFD) and Charge Pump (CP) – CP-PLL – PLL Integer-N Frequency Synthesizer – PLL Divider Chain with Injection-Locked Frequency Divider –Class E (stacked FET and others) Power Amplifiers for 60/77 GHz bands – Doherty Power Amplifier – Project Based Implementation Practices.

Outcomes:

CO1 Ability to design Receiver using LNAs, Oscillators and Mixers.
CO2 Ability to designtransmitterusing Power Amplifiers.
CO3 Course Project on 60 GHz 5G Receiver/Doherty PA design and development in Lab.

TEXT BOOKS / REFERENCES:

1. B Razavi, *RF Microelectronics*, Second Edition, Pearson, 2012 (Indian Edition 2013 by Dorling Kindersley).
2. SorinVoinigescu, *High-Frequency Integrated Circuits*, Cambridge University Press, 2013, South Asian Paperback edition of 2018.
3. Michael Steer, *Microwave and RF Design - A Systems Approach*, SciTech Publishing, 2010, Indian Reprint by Yesdee Publishing, 2012.

4. Thomas H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Second Edition, Cambridge University Press, 2004, Indian Reprint of 2009.

18VL752 COMMUNICATION SYSTEMS AND NETWORKS 3-0-0-3

Objectives:

- To study the basics of sampling and quantization, coding, modulation, signal detection and system performance in the presence of noise.
- To study the data networking concepts including multiple access, reliable packet transmission, routing and protocols of the internet.

Keywords: Digital Modulations, Signal Detection, Multiple Access,

Routing Protocols. **Contents:**

Review of Digital Communication Systems – Sampling – Quantization –Waveform Coding Formats – Pulse Shaping and Matched Filter.

Baseband Modulation Techniques– MPSK, MQAM– Pass Band Modulation Techniques – QAM – Performance of Digital Modulation – AWGN Channels – Fading Channels – Capacity in AWGN Channels and Fading Channels –ErgodicCapacity and Outage Capacity.

Multi user Systems– Sum Rate Capacity– Multiple Access Techniques – TDMA, FDMA, SDMA, CDMA, OFDMA – Interference Limited Systems – Noise Limited Systems– Case Studies and Design Applications.

Outcomes:

CO1 Ability to design a communication system with specific high level constraints.
CO2 Ability to apply the concepts in the context of aerospace communication systems: aircraft communications, satellite communications, and deep space communications.
CO3 Ability to evaluate and assess the performance of communication networks in real time setting.

TEXT BOOKS / REFERENCES:

1. John Proakis and MasoudSalehi,*Digital Communications* , Fifth Edition, McGraw-Hill Publications, 2007.
2. Simon S Haykins, *Digital Communication Systems*, Wiley Publication, 2013.
3. David Tse and PramodVishwanath, *Fundamentals of Wireless Communication*, Cambridge University Press, 2005.
4. Ray Horak, *Communications Systems and Networks*, Third Edition, Wiley Inc., 2002.

TECHNOLOGY

18VL761 NANO ELECTRONICS 3-0-0-3

Objectives:

- To understand the latest trends in the technology and principles of nano-electronics.

- To familiarize new material devices and their performances.

Keywords: Quantum Well, Wire, Graphene, FINFETS, CNT.

Contents:

The Schrödinger Equation –Electrons in a Crystal Lattice – Quantum Well– Wire and Dot Devices – – Phonons and Photons – Scattering Rates and Lifetimes in Electronic Devices –CVD and Other Processes in Fabrication of Nano Devices – Deep Submicron Devices Limits to Scaling –Nano Devices – Quantum Effects– Atomic Scale Parameter Fluctuation –NanoscaleMOSFET –FINFETS – Vertical MOSFETS.

Resonant Tunneling Transistors –Single Electron Transistors –and Spintronics Devices –Atoms–up Approaches – Transport in Molecular Structures – Molecular Systems as Alternatives to Conventional Electronics – Drift Diffusion– Ballistic Transport –NEGF – Molecular Interconnects – Graphene–Carbon Nanotubes and Silicon Nanowire TechnologyDevices and Circuits.

Spintronics– Band-Structure and Transport – Devices – Applications –Innovative Device Architectures (Double–Gate MOS Transistor –Dynamic Threshold MOS Transistor –Gate–all–Around Transistor –Vertical MOS Transistors) –Nano-Scale and Quantum Devices –Single Electron Transistor (SET) – Quantum Wires – Few-Electron Memories–Steep Slope Switches–Tunnel FETS– Quantum Dot Cellular Automata (QCA).

Outcomes:

CO1 Ability to understand the principles of scaling and limitations of silicon based devices and development of nano-electronic devices.

CO2 Ability to use of wave – particle analysis in the development of transport properties.

TEXT BOOKS / REFERENCES:

1. C.P. Poole Jr., and F.J. Owens,*Introduction to Nanotechnology*, Wiley 2003.
2. WaserRanier, *NanoElectronics and Information Technology (Advanced Electronic Materials and Novel Devices)*, Wiley VCH, 2003.
3. K.E. Drexler, *NanoSystems*, Wiley, 1992.
4. John H. Davies,*The Physics of Low-Dimensional Semiconductors*, Cambridge University Press, 1998.

18VL762 VLSI FABRICATION TECHNOLOGY 3-0-0-3

Objectives:

- To understand the scientific principles involved in the fabrication process.
- To introduce the concept of clean rooms and understand the challenges and limitations involved in extending each fabrication process into the nano-era.
- To introduce some new fabrication concepts employed in industry recently.

Keywords:IC Fabrication, Silicon Processing, Crystal Growth, Photo Lithography, Oxidation, Diffusion, Etching, Copper Interconnects, CMOS Technology, Film Deposition.

Contents:

Process Overview – Crystal Growth, Wafer Fabrication, and Basic Properties of Silicon Wafers – Clean Rooms and Wafer Cleaning – Lithography – Light sources, Exposure systems, Resists, Masks – Steps in practical Lithography – Advanced Mask Engineering - Non-optical Lithographic Techniques.

DopantDiffusion – Thermal Oxidation – Oxide growth models – Oxide Characterization – Alternative Gate Dielectrics – Etching – Wet, Plasma, Ion Milling – Reactive Ion Etching – Ion Implantation – Methods and Models – Thin film Deposition – Physical, Chemical and Epitaxial methods.

Process Integration – Back End Technology – Device Isolation – Contacts and Metallization – Silicon Integrated Circuit Process Sequences – CMOS Process – Bipolar Process – MEMS Fabrication.

Outcomes:

CO1 Familiarization with Silicon processing and IC fabrication.

CO2 Clarity on the constraints and modifications needed in extending these processes to nano-era.

CO3 Familiarization with some of the latest techniques used in semiconductor industry.

TEXT BOOKS / REFERENCES:

1. Stephen A. Campbell, *Fabrication Engineering at the Micro- and Nanoscale*, Fourth Edition, Oxford University Press, 2013.
2. Peter Van Zant, *Microchip Fabrication: A Practical Guide to Semiconductor Processing*, Sixth Edition, McGraw-Hill Professional, 2014.
3. James D. Plummer, Michael D. Deal and Peter B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice, and Modeling*, Prentice Hall (Indian edition published by Dorling Kindersly India Pvt. Ltd), New Delhi, 2001.
4. Richard C. Jaegar*, Introduction to Microelectronic Fabrication: Volume 5 of Modular Series on Solid State Devices*, Second Edition, Prentice Hall, 2002.

18VL763 ELECTRONIC PACKAGING AND RELIABILITY 3-0-0-3 Objectives:

- To introduce basic concepts and types in Microchip Packaging.
- To understand how packaging needs vary for various applications.
- To understand the thermal, mechanical, electrical and chemical degradation mechanisms which affect the reliability of packaged devices.
- To make VLSI Design students appreciate the importance of the package design.

Keywords:IC Fabrication, device assembly, packaging, CMOS Technology, flip chip, Ball Grid Array, hermitic package, infant mortality – bath tub curve, radiation hardening, SMT, Monolithic 3D.

Contents:

General Packaging Principles –Wire Bonding – Flip Chip Technologies –Types of Packaging – Ball Grid Array – Quad Lead – Surface Mount Technology –Monolithic 3D.

Component Packaging (Including Integrated Circuits, Opto, MEMS, RF and Solar Devices) – Substrates used in Packaging –Electrical and Thermal Considerations.

Reliability Test Strategies –Reliability Modelling –Reliability Testing, Degradation and Failure Mechanisms – MTTF, FIT, Thermal – Chemical – Electrical and Mechanical –Characterization Techniques.

Outcomes:

CO1 Exposure to various IC packaging techniques.
CO2 Understanding the constraints in each techniques and modifications needed in extending these to various applications.
CO3 Understanding of the reliability issues in packaging.

TEXT BOOKS / REFERENCES:

1. Vasilis F. Pavlidis, IoannisSavidis and Eby G. Friedman, *Three dimensional Integrated Circuit Design*Second Edition., Morgan Kaufmann, 2017.
2. Milton Ohring and Lucian Kasprzak,*Reliability and Failure ofElectronic Materials and Devices*, Second Edition, Academic Press, 2014.
3. ChuanSeng Tan, Kuan-Neng Chen and Steven J Koester, *3D integration for VLSI Systems*,Pan Stanford Publishing, CRC Press, 2012.
4. Andrea Chen and Randy Hsiao-Yu Lo, *Semiconductor Packaging: Materials Interaction and Reliability*, CRC Press, 2012.
5. Richard K. Ulrich and William D. Brown,*AdvancedElectronicPackaging*, John Wiley & Sons, Inc., 2006.

18VL764 MEMS DESIGN AND FABRICATION 3-0-0-3

Objectives:

- Understanding the basics of Micro Electro Mechanical Systems and the processing technologies.
- To understand the concepts and principles of micro sensors, actuators and their fabrication techniques.
- Understand the applications of MEMS in various fields.

Keywords: Microelctronic Technologies, Smart Materials Systems, Micromachining.

Contents:

Introduction to MEMS – MEMS materials – Standard Microelctronic Technologies- Silicon and Polymeric MEMs Fabrication – MEMS and Smart Materials Systems.

Silicon Bulk Micromachining - Silicon Surface Micromachining - Microsensors and Microactuators – Fabrication and Packaging of Smart Microsystems.

MEMS based Sensors and Devices for Satellite Communication – Space Technology – Medical and Aerospace Applications – Wireless Technology – Smart Sensors and MEMS Devices.

Outcomes:

CO1 Able to understand the concept of MEMS based systems and devices.
CO2 Able to understand the applications of MEMS in satellite, space technology, medical and aerospace.

TEXT BOOKS/REFERENCES:

1. Julian W. Gardner, Vijay K.Varadan and Osama O. Awadelkarim, "*Microsensors, MEMS, and Smart Devices",* Wiley, 2001.
2. Jha A. R., "*MEMS and Nano Technology – Based Sensors and Devices for Communications Medical and Aerospace Applications",* CRC press, 2008.
3. Vijay K. Varadan, Vinoy K.J. and Gopalakrishnan S., "*Smart Material Systems andMEMS: Design and Development Methodologies",* Wiley, 2006.
4. Richard Zurawsky, "*Embedded Systems Handbook",* CRC Press, 2006.
5. Steven S. Saliterman, "*Fundamentals of BioMEMS and Medical Microdevices",* SPIE Press, 2006.

FRACTAL ELECTIVES

ANALOG CIRCUITS AND DEVICES

18VL771 ANALOG LAYOUT 1-0-0-1

Objective:

0 To study and practice layouts, and to understand its significance on circuit performance.

Contents:

CMOS IC Design Process-The Well and the Substrate : Patterning, Laying out and Design Rules. N-well Resistor- N-well/Substrate diode-Depletion Layer Capacitance-RC Delay through an N-well Metal, Active and Poly Layers: Design Rules, Layout, Patterning and parasitic. Bonding Pads- Via-Standard Cell Frame-Layout Using Cell Hierarchy. CMOS Transistor Layout: compact, relief stress, gate protection, Close proximity, Guard rings and yield. Verifying the Transistor Layout: DRC and LVS.

Outcomes:

CO1 Design and develop a compact CMOS transistor layouts following the design rules. CO2 Ability to analyse the parasitic associated.

TEXT BOOKS/REFERENCES

1. R. Jacob Baker, Harry W. Li and David E. Boyce, *CMOS circuit design, layout, and fabrication", IEEE series on Microelectronic systems*, ThirdEdition, Wiley 2010.
2. www.eda-utilities.com.
3. B. Razavi, *Design ofAnalog CMOS Integrated Circuits*, McGraw-Hill, 2000.

18VL772 FEEDBACK AMPLIFIERS 1-0-0-1

Objective:

0 To study and analyse the CMOS realization of Feedback amplifiers.

Contents:

Feedback amplifiers - CMOS Realization and analysis – Barkhausen criterion- Stability –Distortion - Voltage / current, series / shunt feedback amplifiers – Effect of loading.

Outcome:

0 Analysis of Feedback amplifiers.

TEXTBOOKS/REFERENCES:

1. Razavi, Behzad. , "*Design of analog CMOS integrated circuits"Mc*Graw-Hill International Edition, 2001.
2. Allen, Phillip E., and Douglas R. Holberg. *CMOS analog circuit design*.Oxford Univ. Press, 2002.

18VL773 ANALOG FILTERS 1-0-0-1

Objective:

- To study and analyze and design analog filters.

Contents:

Bilinear Transfer function and Frequency response- Cascade design with first order circuits- Biquad circuits- Butterworth Filters.

Outcome:

CO1 Ability to design analog filters.

TEXTBOOKS/REFERENCES:

1. Analog Filter Design Author: M. E. Van Valkenburg Edition: 1995 Publisher: Oxford University Press ISBN: 978-0195107340.
2. Allen, Phillip E., and Douglas R. Holberg. *CMOS analog circuit design*.Oxford Univ. Press, 2002.

18VL774 PHASE-LOCKED LOOPS 1-0-0-1

Objectives:

0 To study and understand PLL design and phase noise parameters.

Contents:

A short history of PLLs-Linearised PLL models-Noise properties- Voltage Controlled Oscillators-Sequential Phase detectors- Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators -loop filters and charge pumps-Phase Noise- Synthesizer design examples- DECT applications.

Outcome:

CO1 Ability to design a complete frequency synthesizer and analyse its performance.

TEXT BOOKS/REFERENCES:

1. Thomas H.Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Second Edition, Cambridge University Press, 2004, Indian Reprint of 2009.
2. B. Razavi, *RF Microelectronics*, Second Edition, Pearson, 2012 (Indian Edition 2013 by Dorling Kindersley).

TESTINGAND VERIFICATION

18VL775 BUILT-IN SELF TEST 1-0-0-1

Objective:

- To understand the principles of memory testing.

Contents:

BIST Design Rules - Test pattern generation: – Pseudo-exhaustive pattern generation- Pseudorandom pattern generation – Output Response Analysis: – Syndrome Checking – Signature Analysis - Functional Fault Models and Test Algorithms - Memory Built-In Self-Test - Memory Built-In Self-Repair - Memory Diagnostics - Memory on-Line Testing - Testing Content Addressable Memories - Testing Non-volatile Memories.

Outcome:

CO1 To be able to identify optimum memory testing algorithms for different types of memories.

TEXTBOOKS/REFERENCES:

1. Van de Goor, "Testing *Semiconductor Memories: Theory and Practice*", John Wiley & Sons, Chichester, England, 1991.

COMPUTATIONAL VLSI

18VL776 DEEP LEARNING TECHNIQUES 1-0-0-1

Objective:

0 To develop expertise of the students in deep learning and its applications.

Contents:

Introduction to Artificial Neural Networks (ANNs)-Feedforward neural networks- Gradient descent-backpropagation learning-Stochastic gradient descent-Activation functions-regularization-batch normalization; Convolutional neural networks- Fundamentals-architectures-pooling-visualization;Recurrent neural networks (RNN)-fundamentals- Long-Short Term Memory (LSTM)-architectureand training; Deep generative models-fundamentals-Autoencoders-Architecture and training; case studies.

Outcomes:

CO1 Training the students on the fundamentals of deep learning algorithms.
CO2 Prepare them to apply these algorithms for their further study/research.

TEXT BOOKS / REFERENCES:

1. Ian Goodfellow, YoshuaBengio, AaronCourville, *Deep Learning*, MIT Press, 2016.
2. K. P. Murphy, *Machine Learning: A Probabilistic Perspective*, MIT Press, 2012.
3. Christopher M. Bishop, *Pattern Recognition and Machine Learning*, Springer, 2006.

18VL777 INTERNET OF THINGS 1-0-0-1

Objective:

- To explore the knowledge in Internet of Things – Architecture, Protocols, Hardware and Software Technologies.

Contents:

Introduction to IoT – IoT definition – Characteristics – IoT Complete Architectural Stack – IoT enabling Technologies – IoT Challenges.Sensors and Hardware for IoT – Hardware Platforms – Arduino, Raspberry Pi, Node MCU..

Protocols for IoT – Infrastructure protocol (IPV4/V6/RPL), Identification (URIs), Transport (Wifi, Lifi, BLE), Discovery, Data Protocols, Device Management Protocols. – A Case Study with MQTT/CoAP usage.

Outcomes:

CO1 Hands-on Exposure to Internet of Things Hardware and Software Technologies.

CO2 Both theoretical and practical knowledge in IoT Architecture, Protocols and Applications. **TEXTBOOKS/ REFERENCES:**

1. Pethuru Raj and Anupama C. Raman, *The Internet of Things: Enabling Technologies, Platforms, and Use Cases*, CRC Press, 2017.
2. Adrian McEwen, *Designing the Internet of Things*, Wiley,2013.

RF INTEGRATED CIRCUITS

18VL778 LOW NOISE AMPLIFIER DESIGN 1-0-0-1

Objective:

- To study and understand LNA design and its noise parameters.

Contents:

General Considerations- Problem of Input Matching-Two port noise theory-Intrinsic MOSFET two-port noise parameters- Power-constrained noise figure optimization-LNA Topologies: Common-Source Stage with Inductive Load and Resistive Feedback, Common-Gate and Cascode Stage. Design examples. Gain, noise and stability circles-Variants of Common-Gate LNA - Noise-Cancelling LNA - Reactance-Cancelling LNAs-IIP3 improvement-Differential LNAs.

Outcome:

CO1 Ability to design power constrained noise optimized LNA and to analyse its parameters.

TEXT BOOKS/REFERENCES:

1. Thomas H.Lee, The*Design of CMOS Radio Frequency Integrated Circuits*, Second Edition, Cambridge University Press, 2004, Indian Reprint of 2009.
2. B. Razavi, *RF Microelectronics*, Second Edition, Pearson, 2012 (Indian Edition 2013 by Dorling Kindersley).

18VL779 OSCILLATOR DESIGN 1-0-0-1

Objective:

- To study, design and analyze CMOS oscillator.

Contents:

Oscillation criteria – CMOS oscillator design – Operation and analysis of RC phase shift, Ring Oscillator, Wienbridge, Hartely, colpitts, crystal Oscillator – Quadrature Oscillator - VCO .

Outcome:

CO1 Ability to design CMOS based oscillators.

TEXTBOOKS/REFERENCES:

1. Razavi, Behzad. , *Design of analog CMOS integrated circuits,Mc*Graw-Hill International Edition, 2001.
2. Allen, Phillip E., and Douglas R. Holberg. *CMOS analog circuit design*.Oxford Univ. Press, 2002.

18VL780 SIGNAL INTEGRITY 1-0-0-1

Objectives:

- Establish a sound basis for signal and power integrity design rules.
- Understanding 3D electromagnetic simulation.

Contents:

Introduction to Signal Integrity – Power and frequency spectrum- phase/amplitude response of linear systems – signal distortion – time domain reflections – impedance matching considerations – noise, electromagnetic coupling and interference (EMI)- fast time domain measurements.

Outcome:

CO1 Knowledge of pitfalls in high frequency design.
CO2 Efficient design for board level interface.

TEXT BOOKS/REFERENCES:

Thierauf, Stephen C. *Understanding signal integrity*. Artech House, 2010.

TECHNOLOGY

18VL781 FINFET ARCHITECTURE 1-0-0-1

Objective:

- Understand the importance of non conventional MOSFET structures

in VLSI. **Contents:**

SOI Technology – FINFET structure – Design – Fabrication –Physics and Operation - Performance and Issues- FINFET vs CMOS – Applications.

Outcomes:

CO1 Design and simulate FINFET based circuits
CO2 Ability to use prototyped systems for various applications

TEXT BOOKS/REFERENCES:

1. Yogesh Singh Chauhan, Darsen Lu and SriramkumarVenugopalan ,*FINFETModeling for IC simulation and Design* :*Using BSIM-CMG Standard*, First Edition,Elsevier, 2015.

18VL782 GALLIUM NITRIDE DEVICES 1-0-0-1

Objective:

- To study the characteristics of GaN devices and the processing challenges ahead in the development of novel devices.

Contents:

III-V Nitrides for Device Applications- GaN Physical and thermal properties- Substrate and materials-Lateral and vertical GaN technology- Processing Challenges for Novel Electronics – Electrical characterisation- Optical characterisation – Modelling GaN HEMT devices-GaN based nanotubes and nanowires.

Outcome:

CO1 Ability to model, characterise and develop GaN based HEMT devices and nanotubes.

TEXT BOOKS/REFERENCES

1. MatteoMeneghini, GaudenzioMeneghesso and Enrico Zanoni (Editors), *PowerGaN devices : Materials, Applications and Reliability*, Power Electronic and power system series, Springer International publishing, 2017.
2. www.cree.com/.